CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:

executing at a processor core module of a system on a chip (SOC) a first MSR access command, the first MSR access command comprising a first destination address and a first destination data; and

providing, in response to executing the first MSR access command, a first access request to an external bus port to access an external device, the first access request including the first destination address and the first destination data and the external device being external the SOC.

2. (Original) The method of claim 1 further comprising:

providing, in response to executing the first MSR access command, a second access request including the first destination address and the first destination data to a bus interface module, wherein the bus interface module is part of the SOC; and

wherein providing the first access request is further based on providing the second access request to the bus interface module.

3. (Original) The method of claim 2, further comprising:

providing, in response to providing the second access request, a third access request including the first destination address and the first destination data to a peripheral interface module, wherein the peripheral interface module is part of the SOC; and

wherein providing the first access request to the external bus port further comprises the peripheral interface module providing the first access request.

4. (Original) The method of claim 3, wherein the second access request includes providing the second access request to a first bus coupling the processor core module to the bus

interface module and wherein the third access request includes providing the third access request to a second bus coupling the bus interface module to the peripheral interface module.

5. (Currently Amended) The method of claim 3 further comprising:

executing at the processor core a ~~second~~ set of MSR access commands, the ~~second~~ set of MSR access commands comprising one or more MSR access commands; and

configuring, in response to executing the ~~second~~ set of MSR access command, at least a portion of the bus interface unit.

6. (Original) The method of claim 5 wherein configuring further comprises address information to prevent a memory location associated with the first destination address from being accessed in response to a memory access command.

7. (Original) The method of claim 6, wherein the address information comprises address mapping information.

8. (Original) The method of claim 6, wherein the address information comprises address masking information.

9. (Original) The method of claim 6 wherein configuring further comprises defining the memory map to prevent the memory location associated with the first destination address from being accessed in response to an IO access command.

10. (Original) The method of claim 5 wherein configuring further comprises defining a memory map to prevent a memory location associated with the first destination address from being accessed in response to an IO access command.

11. (Original) The method of claim 1, wherein providing the first access request to the external bus port further comprises a peripheral interface module providing the first access request.

12. (Original) The method of claim 1 further comprising:

accessing a first external peripheral when the first destination address has a first value; and

accessing a second external peripheral when the first destination address has a second value.

13. (Original) A system comprising:

a processor core portion to decode an MSR write command;

a first interconnect path to provide an address associated with the MSR write command from the processor core to a first external port; and

a second interconnect path to provide data associated with the MSR write command from the processor core to a second external port.

14. (Currently Amended) The system of claim 13 further comprising:

[[a]]the processor core portion to decode an MSR read command;

a third interconnect path to provide an address associated with the MSR read command from the processor core to a third external port; and

a fourth interconnect path to provide data associated with the MSR write command to the processor core from a fourth external port.

15. (Original) The system of claim 14, wherein the second external port and the fourth external port are the same port.

16. (Original) The system of claim 15, wherein the first external port and the third external port are the same port.

17. (Original) The system of claim 16, wherein the first external port and the second external port at are mutually exclusive.

18. (Original) The system of claim 16, wherein the first external port and the second external port comprise common output nodes.

19. (Original) The system of claim 13 further comprising:

a bus interface unit comprising a first portion of the first interconnect path and a first portion of the second interconnect path.

20. (Original) The system of claim 19 further comprising:

a peripheral interface module comprising a second portion of the first interconnect path and a second portion of the second interconnect path.

21. (Original) The system of claim 13 further comprising:

a first external device coupled to the first external port and the second external port.

22. (Currently Amended) The system of ~~claim 13~~claim 14 wherein the first external device is coupled to the third external port and the fourth external port.

23. (Original) The system of claim 21 further comprising:

a second external device coupled to the first external port and the second external port.

24. (Currently Amended) A system comprising:

a means for executing at a first MSR access command, the first MSR access command comprising a first destination address and a first destination data; and

a means for providing, in response to executing the first MSR access command, a first access request to an external bus port to access an external device, the first access request including the first destination address and the first destination data and the external device being external the SOC.